High-Speed Digital class using Keysight ADS software

Date: Saturday, 2nd March 2024

Venue: Digital University Kerala

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Why is high-speed digital design important?

When digital signals reach gigabit speeds, unpredictability becomes the norm. Potential Signal Integrity issues require evaluation throughout all stages of your project. The process of getting your design back on track starts with the best tools for the job. Keysight's high-speed digital solution set is a range of essential tools, for both measurement and simulation that will help you cut through the challenges of gigabit digital designs. Our tools provide views into time and frequency domains revealing underlying problems and ensuring compliant designs. With Keysight, you'll be equipped to pinpoint problems, optimize the design, and deliver on time.

Software used: Keysight Pathwave ADS v2024

Venue: Digital University, Trivandrum.

Timings: 9:30 AM to 4 :00 PM

Hands-on workshop (License will be provided. Kindly bring laptop)

Registration Fees: Free

Duration: 1 day

Registration Link: REGISTER HERE

Audience

Designers interested in understanding how to design pre-layout with ADS, to use Channel Simulation, IBIS-AMI models, to import board from other PCB tools and to analyze in ADS in post-layout phase with electromagnetic models (EM model).

This training class is designed primarily for SI/PI/HSD engineers.

Electrical Engineers, Digital Design Engineers, Hardware Engineers, Signal Integrity Engineers, Power Integrity Engineers, FPGA Engineers.

Pre-requisites

Good understanding of time-domain simulation

Topics covered:

- Basics of High Speed design & challenges
- Transient simulation
- Pre-layout channel simulation

- Waveform capturing
- Circuit Optimization
- Measure Insertion Loss(IL), eye diagram, Bathtub curve
- Channel Simulation using IBIS-AMI
- COM Simulation
- PAMn simulation
- End to End Channel simulation
- Back channel Interface with IBIS-AMI
- Create a substrate
- Import layout data using odb++
- Power aware signal analysis using SI Pro / Post-Layout EM extraction
- Generate an EM-accurate model that captures signal net losses and coupling
- Frequency domain s-parameter results
- Time domain TDR results
- Controlled impedance line Designer
- Via Designer using FEM simulation

For any further queries, contact:

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